

ATAL Technical Talk



Advancing Semiconductor Reliability: Device Aging and Test Methodologies for Logic Circuits

Yen-Chieh Kevin Huang,

Technical Advisor, Device Dynamics Lab, Taiwan

<https://www.kevinhuang.tw/>

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~2yrs



12yrs



NORDIC
SEMICONDUCTOR

3yrs



Device Aging and Test Methodologies for Logic Circuits

A Quick and Dirty Rundown for Reliability Engineers

Research Motivation and Objectives: lookahead of reliability margin during R&D

- Key Challenges in Semiconductor Reliability:
 - How to correlate discrete transistor aging model to the real application, when there's no “product” yet.
- Reduce iteration cycle time:
 - New technology development delay due to overkill is expensive.
 - Need a practical way to provide confidence on material selection and process change.

Discrete Device Model for Circuit Simulation?

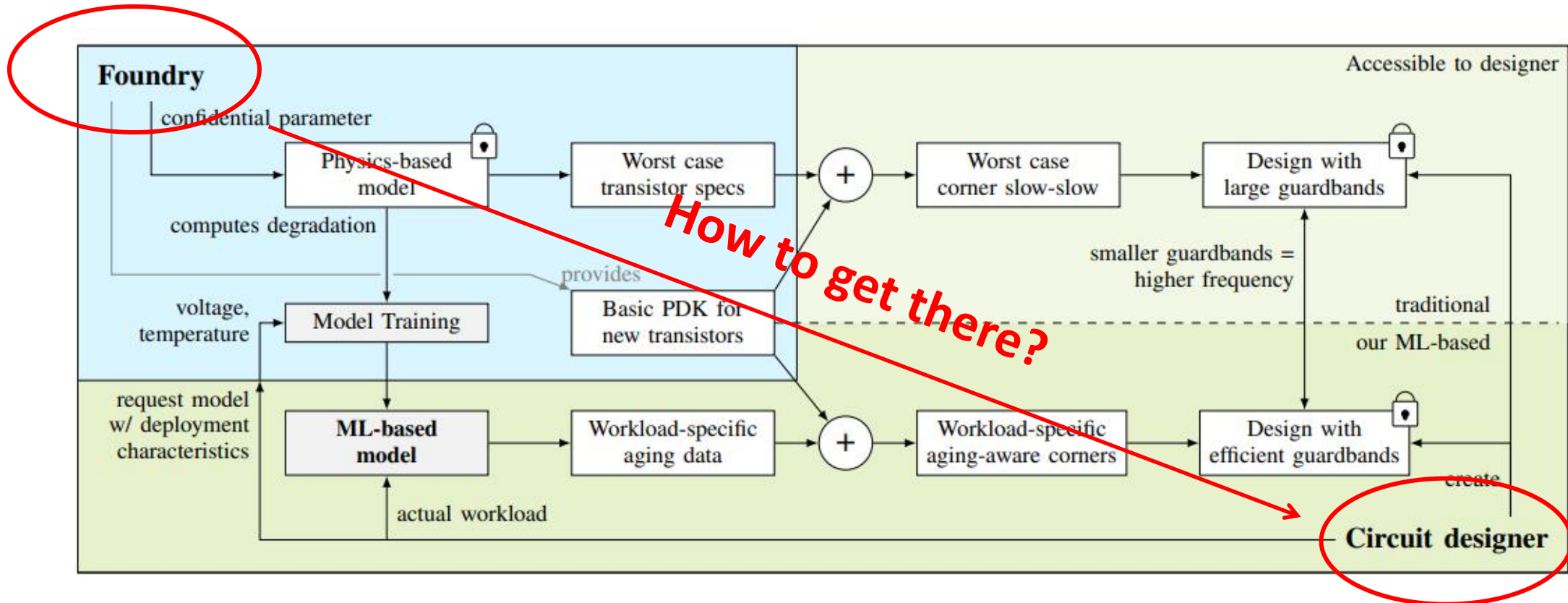
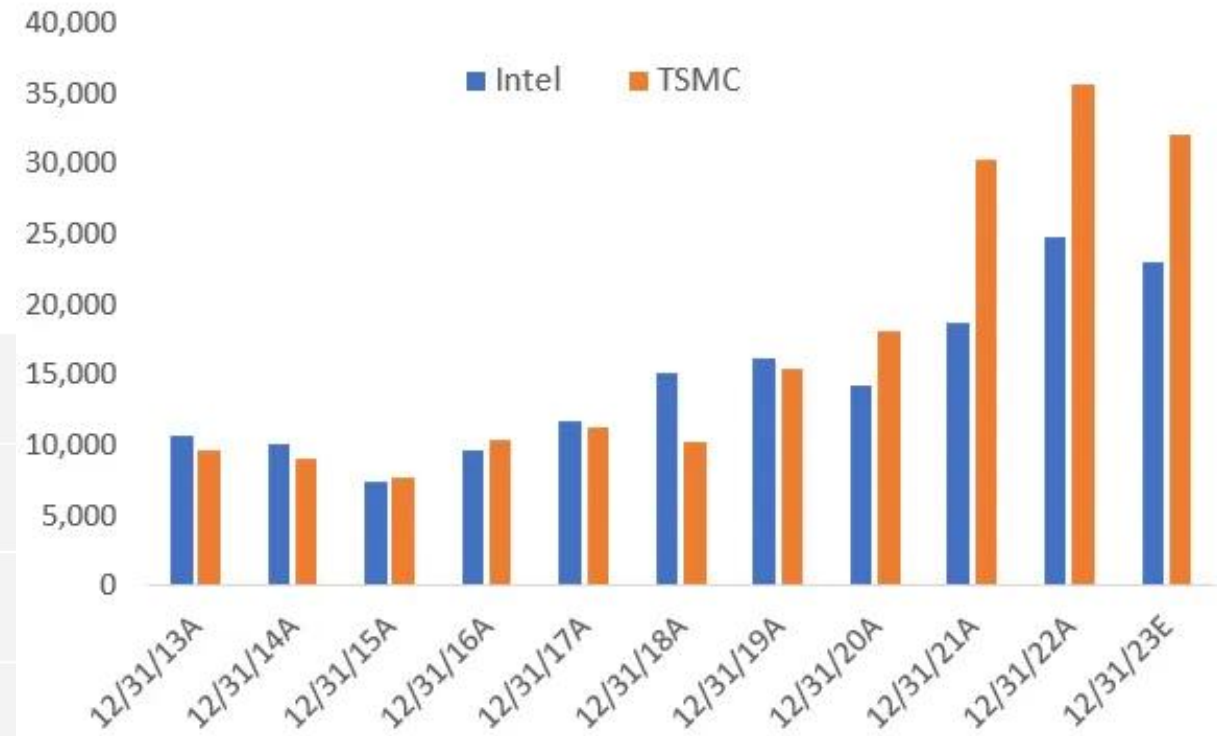


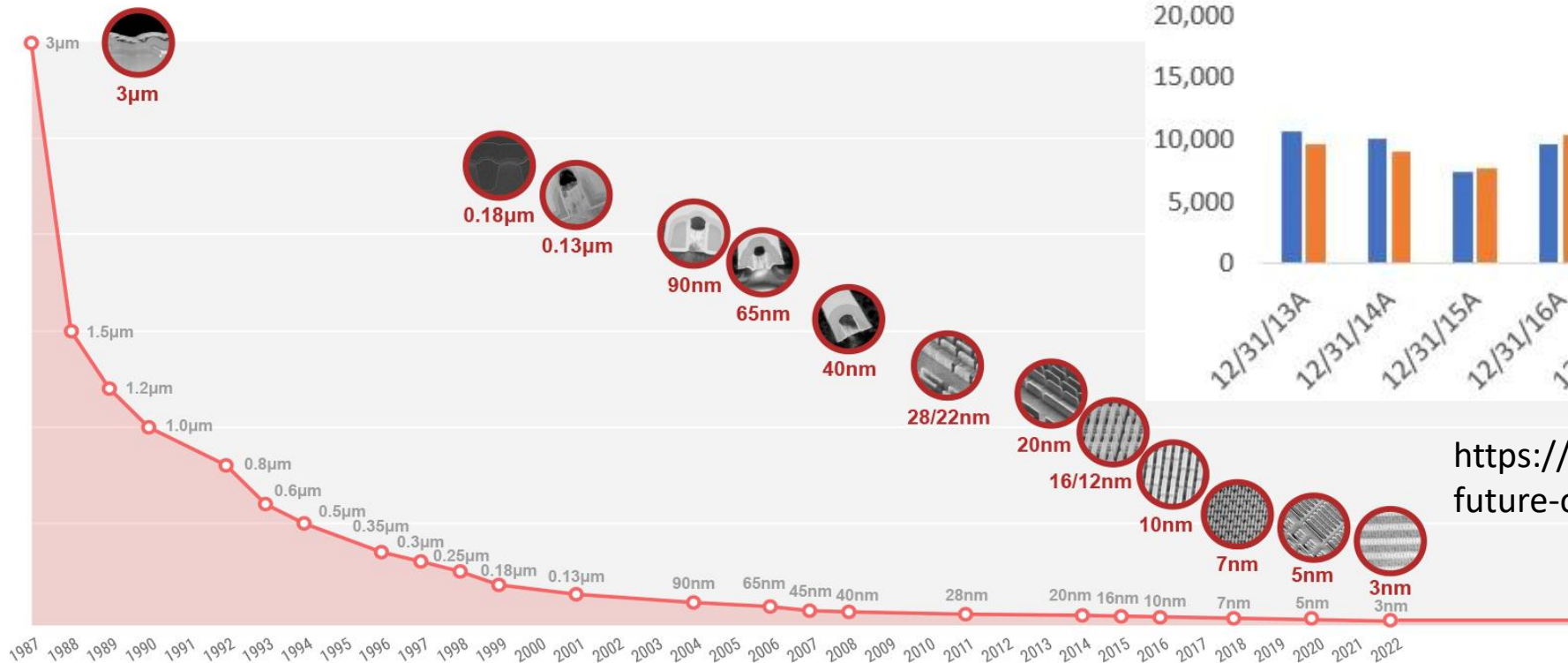
Fig. 2. Typically, circuit designers do not have access to accurate physics-based aging models to estimate efficient (i.e., small, yet sufficient) guardbands. A machine learning-based aging model are free sensitive material and process parameters of the foundry and can thus be shared with designers. Now, circuit designer can create workload-specific aging data for efficient guardbands.

One Iteration Costs More Than A Billion \$

Intel vs TSMC capex (USD billions)



<https://techovedas.com/tsmc-4-trends-shaping-future-of-chipmaking-in-the-next-decade>



Strike the Balance

- **No escape**
 - Hard failure vs Soft failures
- **You shall not overkill**
 - Estimating the acceptable failure rate
- **Mass manufacturing mindset**
 - Statistical meaning with limited (engineering) samples

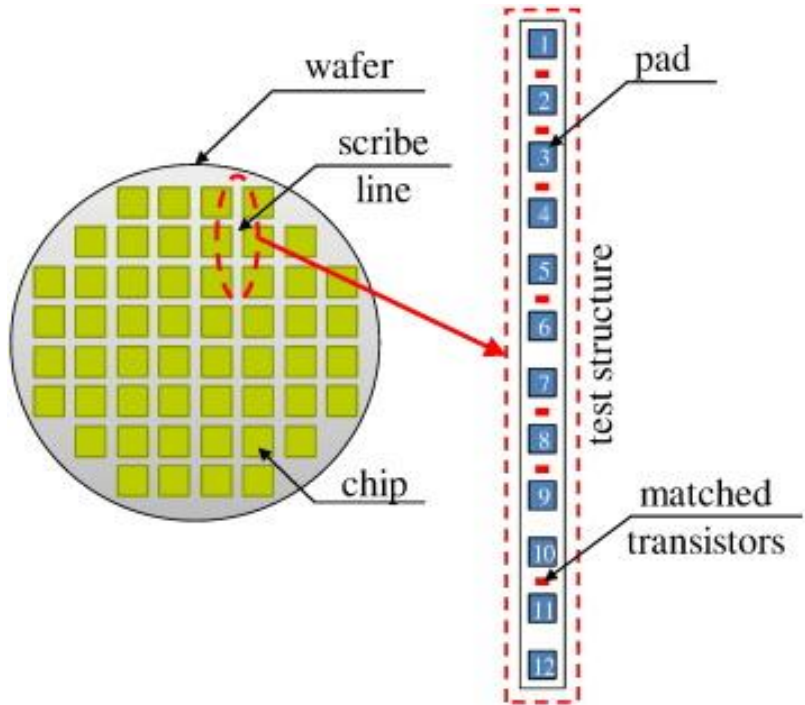


Key Contributions:

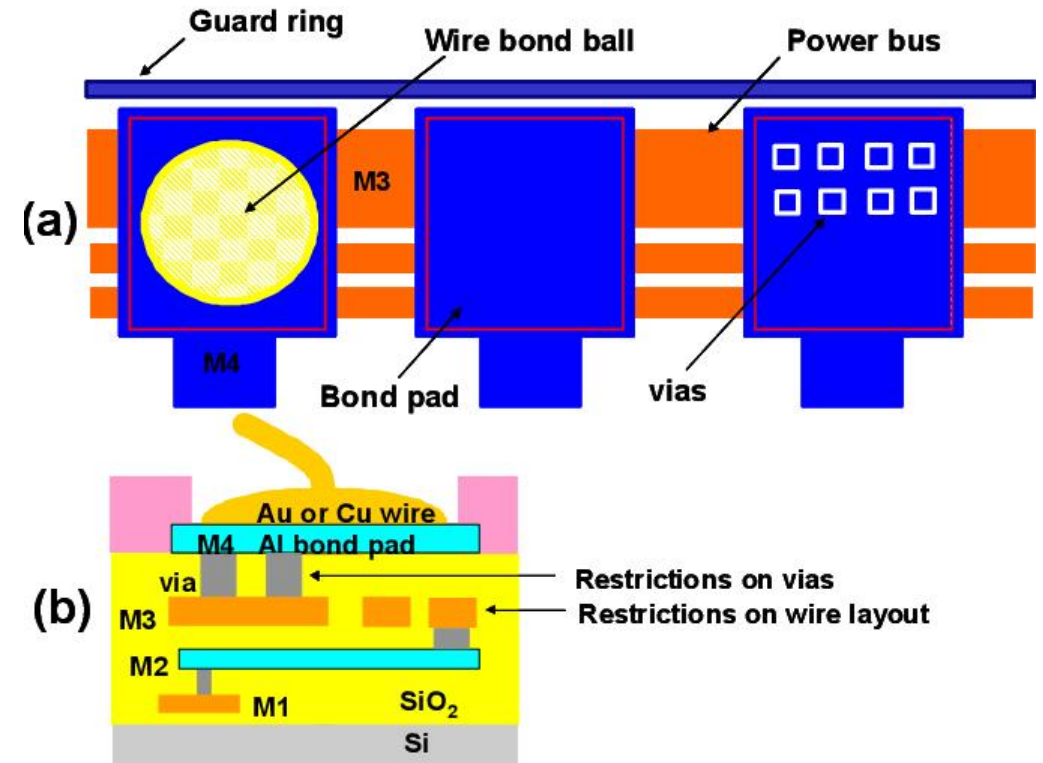
- Focus Areas (to mimic logic circuit operations):
 - Gox oxide breakdown within inverters
 - High frequency (>10MHz) stress
 - Sub-microsecond BTI recovery
- Innovative Test Structures on a testline (scribe line):
 - Test arrays, x10 more throughput
 - Use dedicated circuits to stress a single device
 - Explore sub-microsecond measurements for realistic delay effects

Real Estate is Expensive

All circuit blobs are squeezed on a scribe line

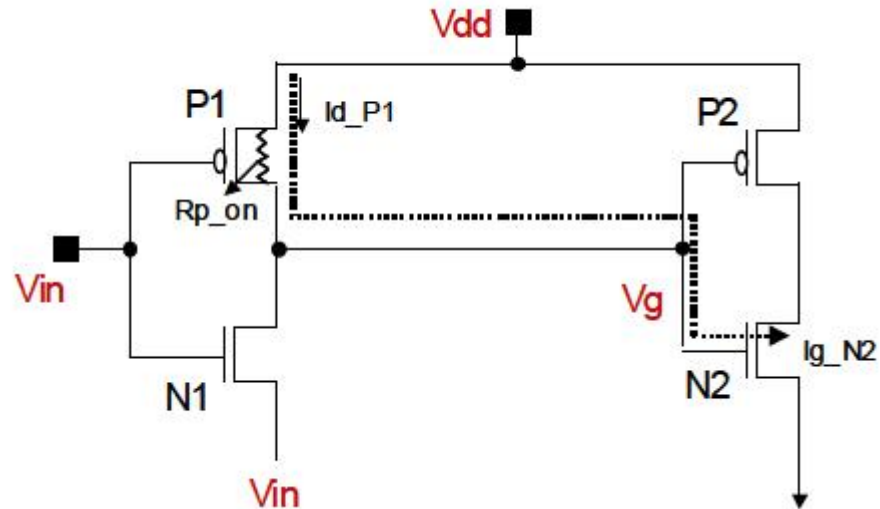


Signal lines routed under pads

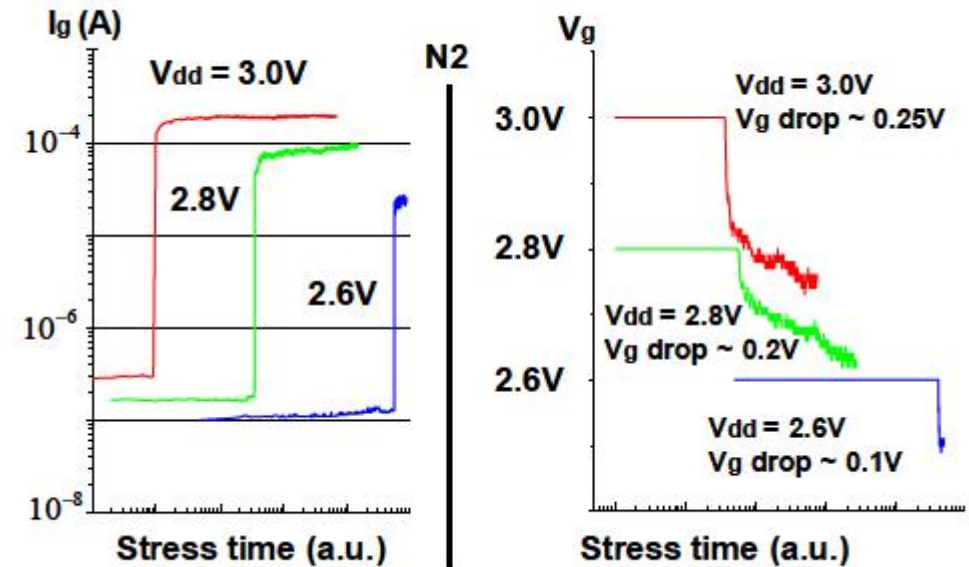


Example: Self-clampping of TDDB

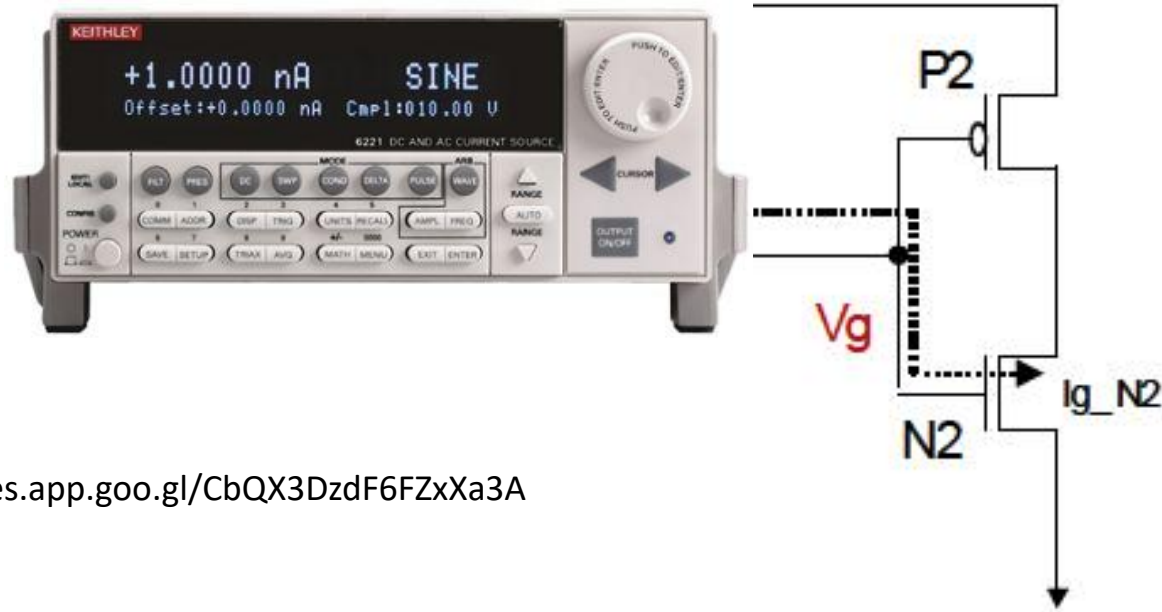
- Transistors are not stand alone, they are connected to each other
 - Stress source is not externally provided with brutal force
 - Inverter: my input is your output, and there's IR drop



Implication?



- No IR drop, prone to hard breakdown



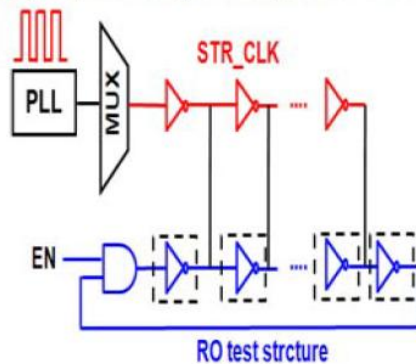
<https://images.app.goo.gl/CbQX3DzdF6FZxXa3A>

Example: Built-in AC Stress (1/2)

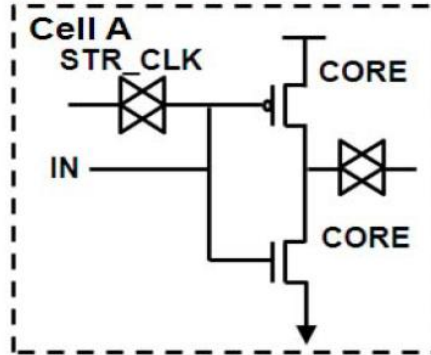
- No huge load from Pads, high frequency is achievable
 - Stress and Measurement modes can be selected externally

Implication?

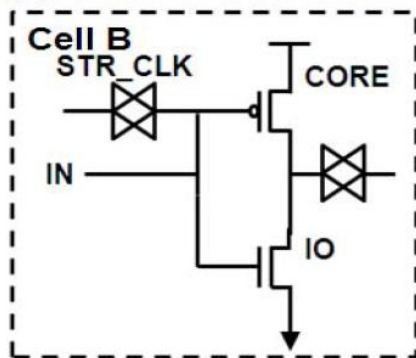
(a) Specially designed RO



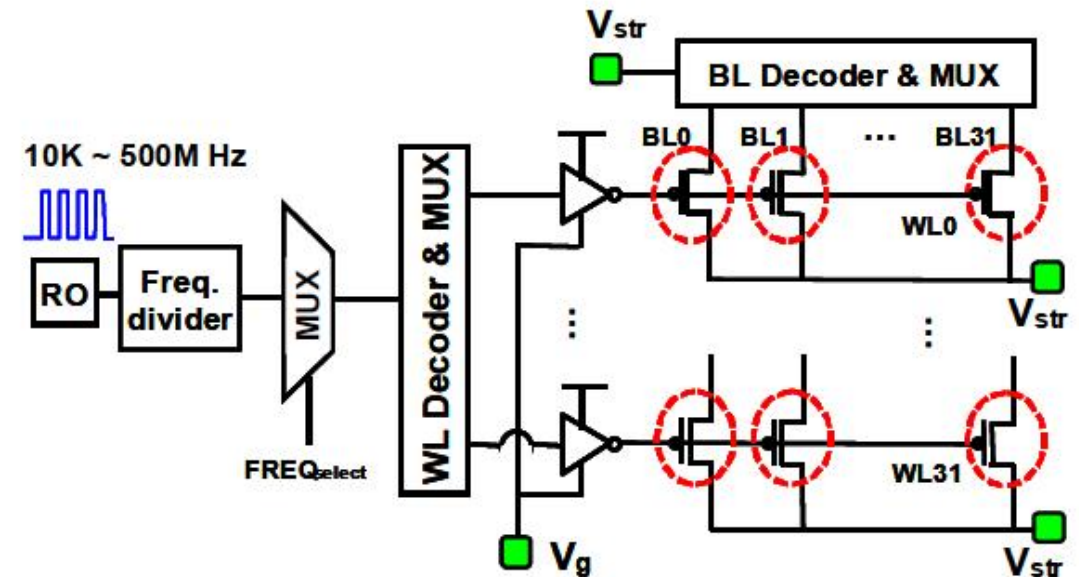
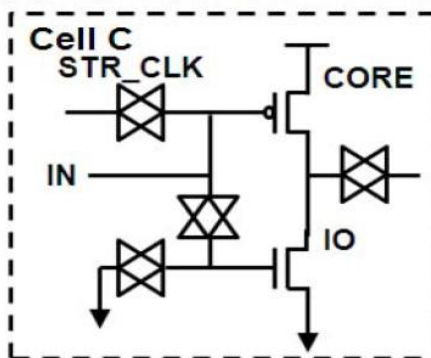
(b) Conventional inverter



(c) Mixed core/IO inverter



(d) Modified core/IO inverter



TDDB

Frequency Shifts

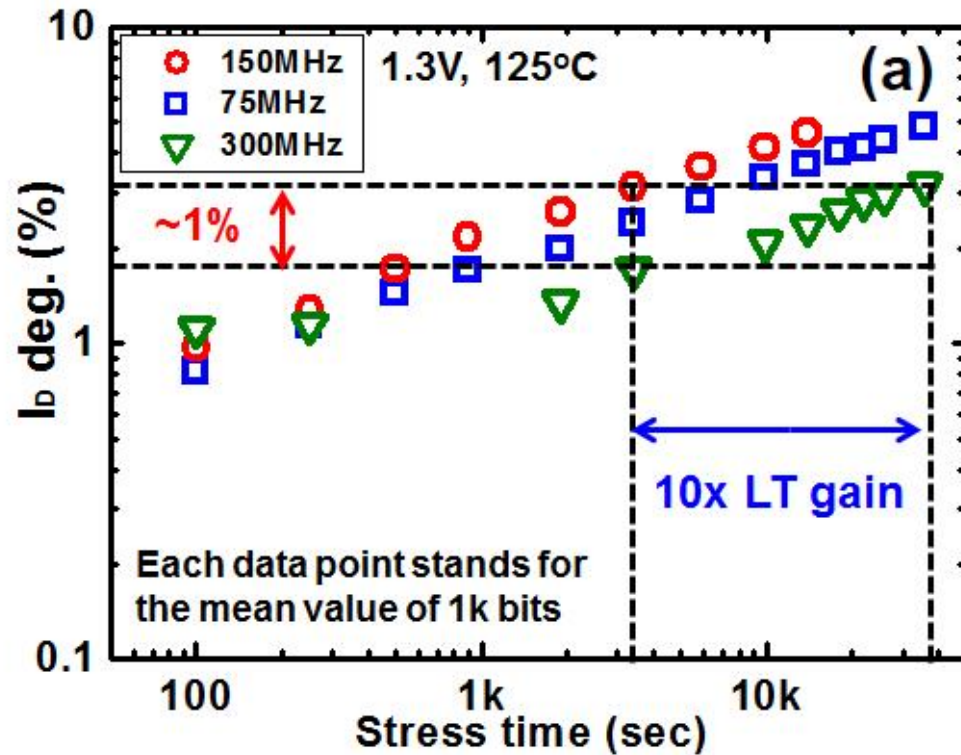
IRPS 2015 6A.4

IRPS 2014 2D.6

Example: Built-in AC Stress (2/2)

- New found reliability margin under AC stress
 - Old method used 1MHz data to predict AC aging

Things to think...



IRPS 2015 6A.4

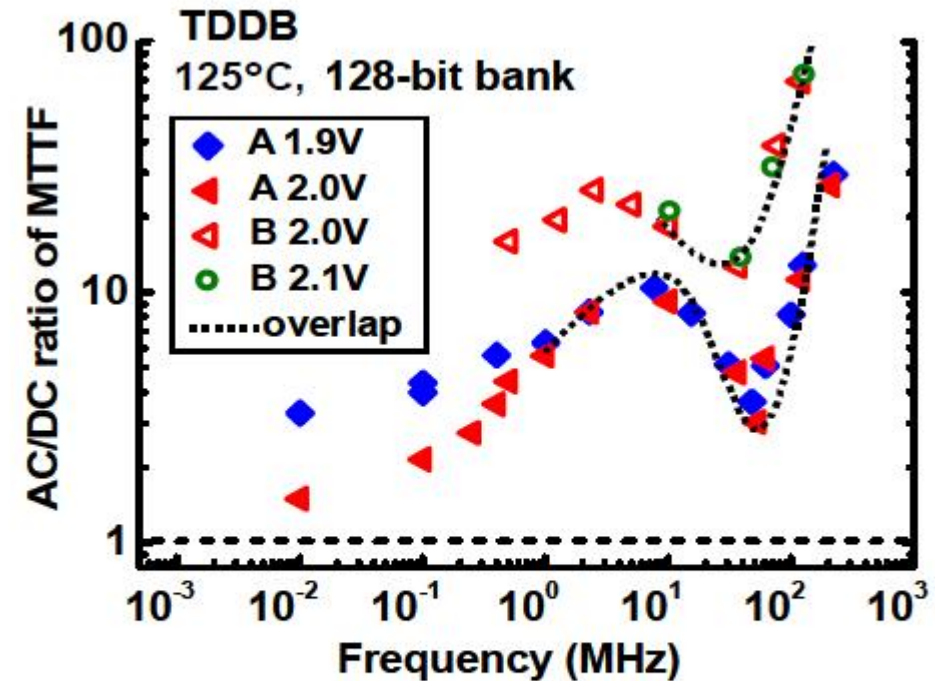


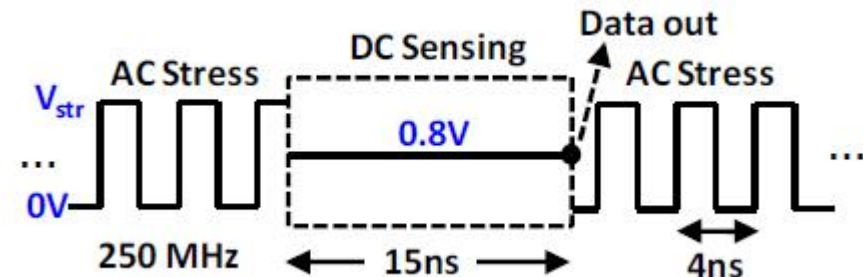
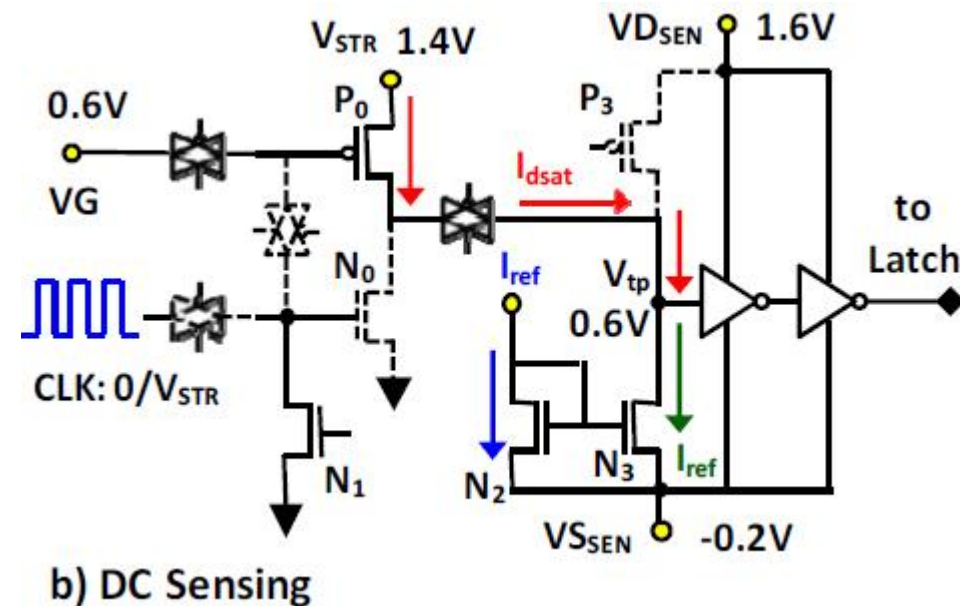
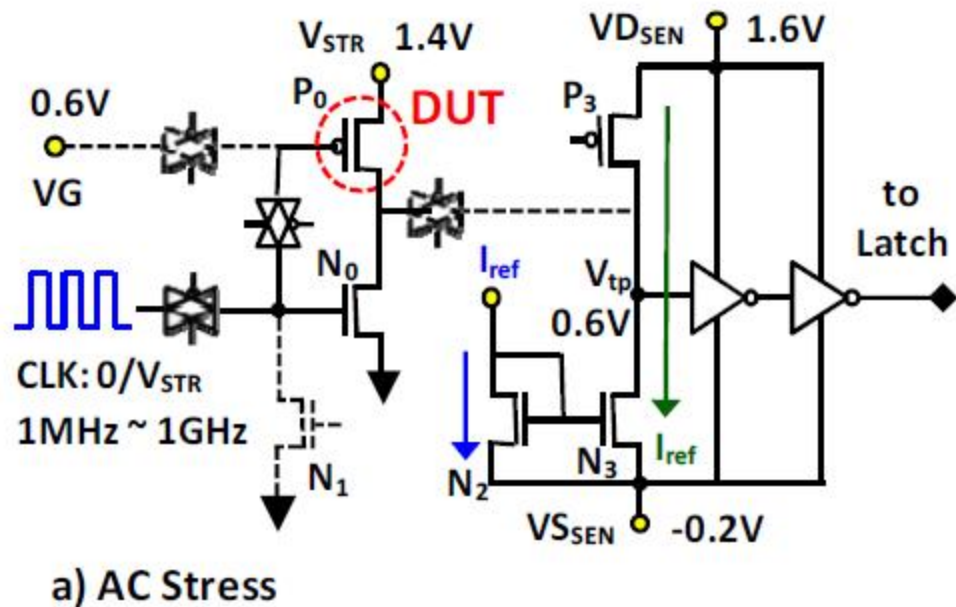
Fig. 4. AC/DC TDD lifetime ratio at high frequencies. Different process (A, B) will have its unique S-shape dependence. In this experiment, process B has longer DC lifetime and larger AC/DC ratio. Each point represents MTTF of a 128-bit bank.

IRPS 2014 XT.3

Example: Sub-microsecond BTI (1/2)

- Using circuits to measure one DUT
 - Current sensing can be done in less $1\mu\text{s}$

Implication?



Example: Sub-microsecond BTI (2/2)

- More than half of the recovery occurs within $1\mu\text{s}$
 - Is BTI really a concern for high speed circuits?

Things to think...

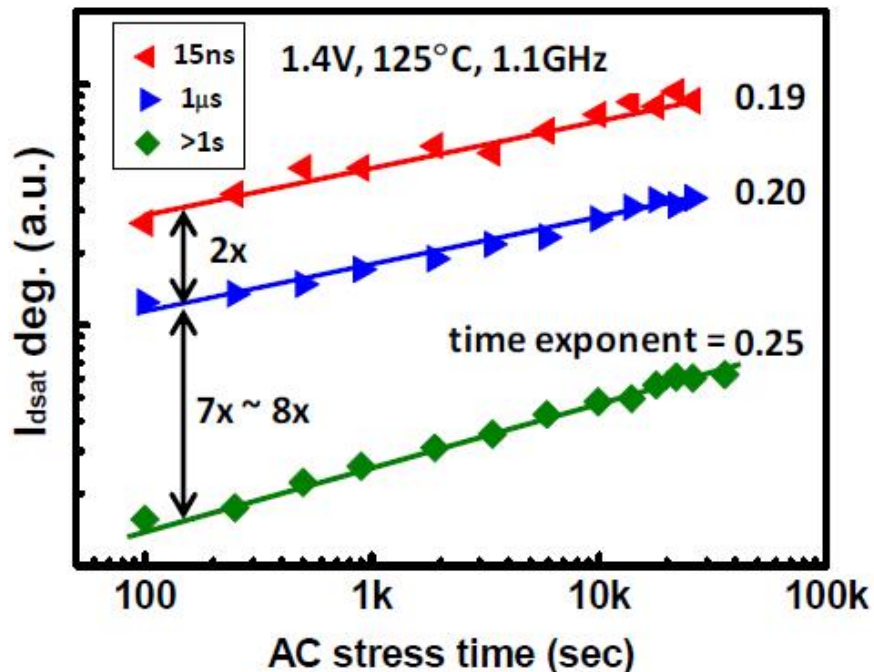


Figure 4. Considerable more degradation can be observed with shorter delay time. Larger time exponent for long delay time is in accordance with relaxation of time zero measurement or *delay artifacts* [13]. Note that a large chunk of degradation, e.g. half at 1.1GHz, recovered within $1\mu\text{s}$.

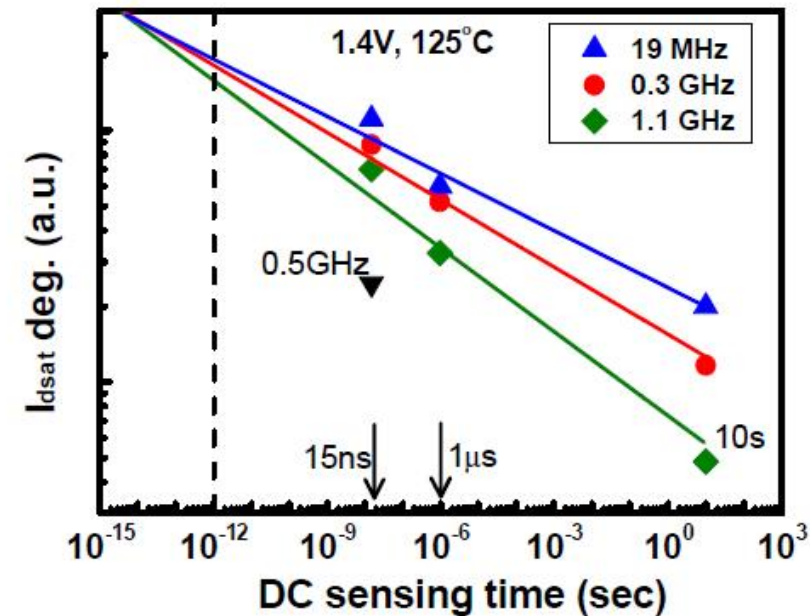


Figure 5. I_{dsat} degradation versus DC sensing time for AC stresses (1.4V, 125°C) at frequencies 19MHz, 0.3GHz, and 1.1GHz. Each data point corresponds to mean value of several measurements. Despite the frequency dependence, total degradations at different frequencies are getting closer at the end of short sensing time. The convergent point for degradation is close to 1fs. Operation faster than 500GHz (with 1ps half cycle) is regarded as far beyond the typical operation speed of most logic circuits.

Our First Structure: Get more data with limited time and wafers

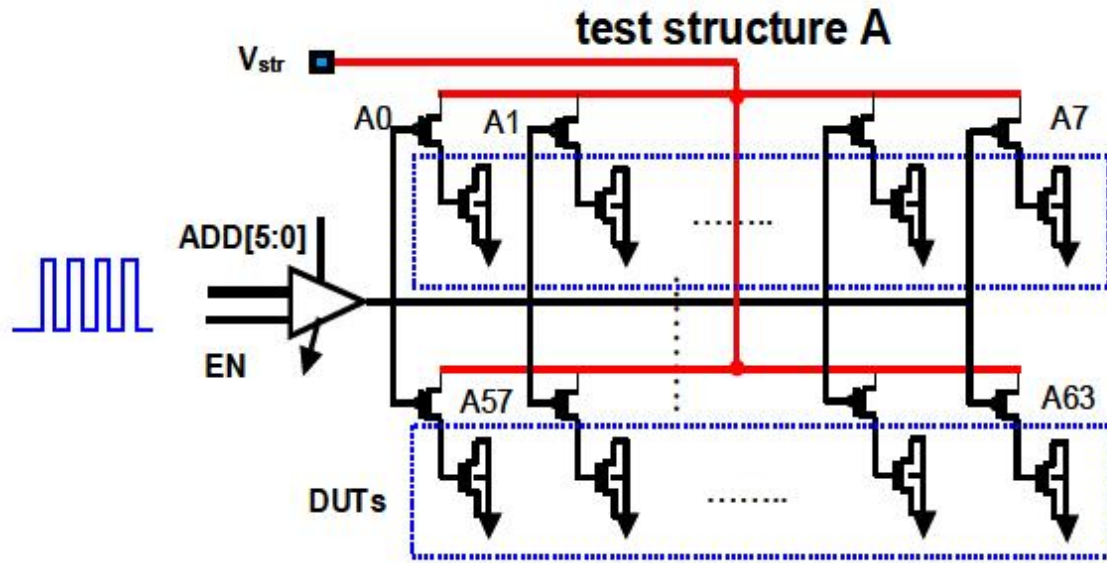
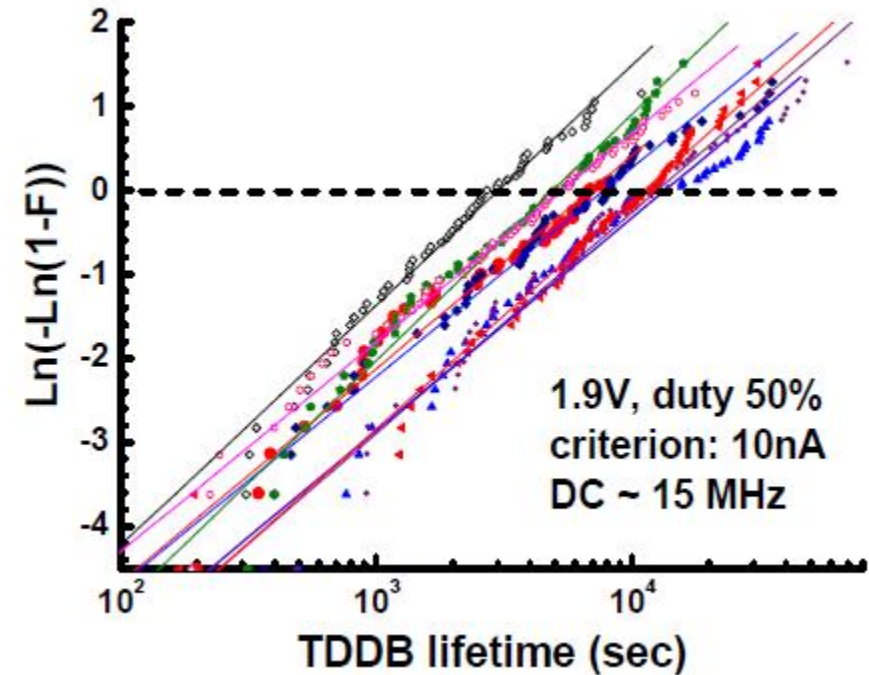


Figure 1. Test array for on-chip DC and AC TDDDB consists of a decoder, EN signal control logic and limiting devices. External AC signal is connected to EN rather directly on the gates of DUTs themselves. This assures a much neater waveform with minimum distortions. During AC stress there is one selected DUT under DC stress as reference bit. Current clamp transistors (PMOS) are fabricated using IO devices to ensure their immunities from high voltage stress.



Example: Test Array

- Mind the control and the routing of Stress and Measurement paths

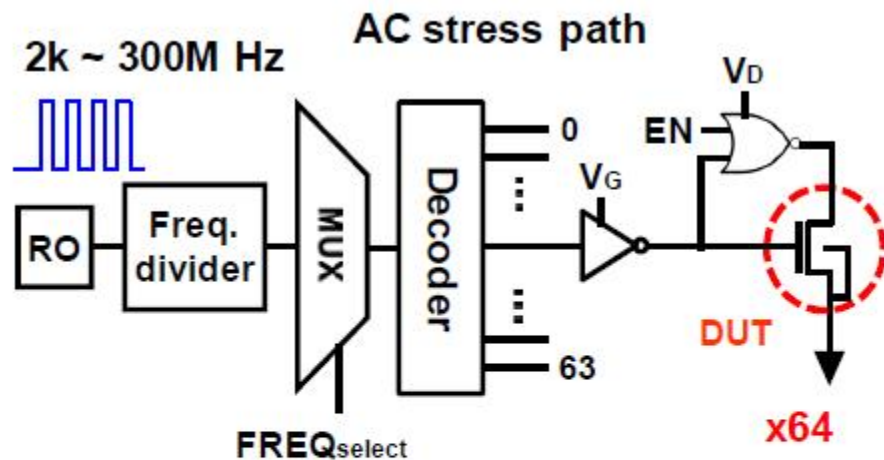
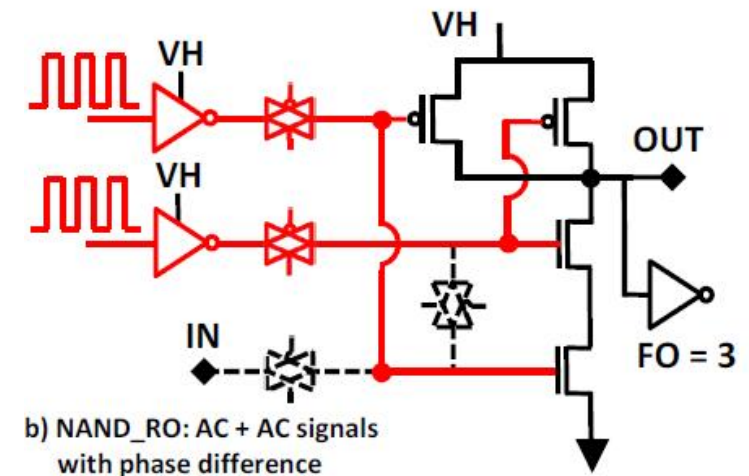
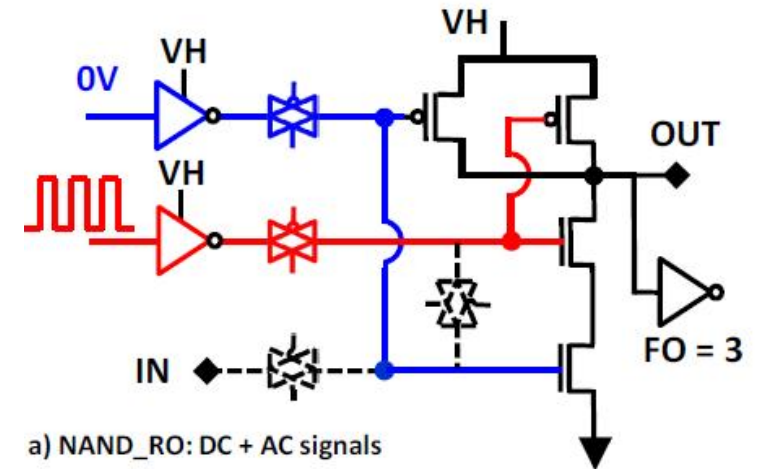


Figure 1. Test array for NMOS TDDDB consists of a built-in ring oscillator (RO) and a 64-DUT mini array. RO is made of thick oxide devices to provide high voltage AC signals on each DUT simultaneously. EN pin selects either conventional (EN=H) or inverter-like (EN=L) stress mode. Drain voltage dependence can be established by setting VG and VD separately.

NMOS TDDB Array

IRPS 2015 GD.1



NAND Array is a Ring Oscillator

Methodology Highlights and Recaps

- Inverter and Ring Oscillator:
 - The interaction between inverter stages plays important roles.
- AC Stress:
 - Built-in on-die high frequency stress source to simulate real-world operating conditions.
 - Internal sensing to capture recovery behavior within 1 μ s
- Test Array:
 - TDDB
 - Ring oscillator for frequency shift

Some Design Tricks

- Always follow design rules unless it's for stress purposes
 - Circuit under pad to route more DC control signals
 - Be extra conservative with post-sim, especially for high speed signal
- Use robust devices for stress source and measurement precision
 - High speed oscillator: longer channel core devices
 - Current mirror: IO devices
- The interface
 - IO device for control and stress immunity
 - Ideally, only the DUT is core device
 - Buffer for outputs
 - Protection diodes for the Pads

Testing the Reliability of My Parachute...

- Everyone has the potential. Sometimes you need to take the plunge.

Questions?

